REMARKS/ARGUMENTS

Claims 1, 2, 6, and 26-48 are pending in the present application. Claim 32 is amended. Reconsideration of the claims is respectfully requested.

I. Examiner Interview

An Examiner Interview was held on March 17, 2008, between Examiner Vu and the undersigned attorney. Suggestions of overcome the present rejections and objections were discussed. No specific agreement was reached.

II. Double Patenting

II.A Claims 1, 32, and 41

The Examiner has provisionally rejected claims 1, 32, and 41 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 6, 21, and 25 of co-pending Application No. 10/675,777 (hereinafter '777).

Applicants acknowledge that this is a provisional rejection. As of the date of this response, neither the rejected claims, nor the claims of the co-pending application have been allowed. Therefore a terminal disclaimer would be premature at this point. Should the Examiner indicate that either the rejected claims, or the reference be allowable, a terminal disclaimer will be filed at that time.

II.B. Claims 1, 32, and 41

The Examiner has provisionally rejected claims 1, 32, and 41 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 2, 10, and 20 of co-pending Application No. 10/675,778 (hereinafter '778).

Applicants acknowledge that this is a provisional rejection. As of the date of this response, neither the rejected claims, nor the claims of the co-pending application have been allowed. Therefore a terminal disclaimer would be premature at this point. Should the Examiner indicate that either the rejected claims, or the reference be allowable, a terminal disclaimer will be filed at that time.

II.C. Claims 1, 32, and 41

The Examiner has provisionally rejected claims 1, 32, and 41 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 3, 17 of co-pending Application No. 10/675,872 (hereinafter '872).

Applicants acknowledge that this is a provisional rejection. As of the date of this response, neither the rejected claims, nor the claims of the co-pending application have been allowed. Therefore a terminal disclaimer would be premature at this point. Should the Examiner indicate that either the rejected claims, or the reference be allowable, a terminal disclaimer will be filed at that time.

II.D. Claims 6, 34, 43

The Examiner has provisionally rejected claims 6, 34, 43 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 4, 12, and 20 of co-pending Application No. 10/675,721 (hereinafter '721).

Applicants acknowledge that this is a provisional rejection. As of the date of this response, neither the rejected claims, nor the claims of the co-pending application have been allowed. Therefore a terminal disclaimer would be premature at this point. Should the Examiner indicate that either the rejected claims, or the reference be allowable, a terminal disclaimer will be filed at that time.

II.E. Claims 1, 32, and 41

The Examiner has provisionally rejected claims 1, 32, and 41 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 12, 23 of co-pending Application No. 10/682,385 (hereinafter '385).

Applicants acknowledge that this is a provisional rejection. As of the date of this response, neither the rejected claims, nor the claims of the co-pending application have been allowed. Therefore a terminal disclaimer would be premature at this point. Should the Examiner indicate that either the rejected claims, or the reference be allowable, a terminal disclaimer will be filed at that time.

III. <u>Objection to the Disclosure</u>

The Examiner objects to the disclosure due to perceived informalities.

Specifically, the Examiner states the following:

> The disclosure is objected to because of the following informalities: The disclosed 'instruction cache' amounts to a language that cannot be accepted due some lexicographic inconsistency, in regard to one of ordinary skill in the useful arts. The disclosure describes functionality being performed by this 'instruction cache', and that appears non-commensurate with known concept, especially when this functionality is not provided with implementation specifics in the Disclosure that would reasonably confirm that a cache is not solely a storage entity but possesses processing intelligence with it. That is, the Specifications teaches 'when instruction cache 300 determines that . . . '(pg. 23, middle); 'process . . . Figure 11 . . . implemented in an instruction cache' (pg. 32, top); 'process . . .

> Figure 12 . . . implemented . . . in an instruction cache' (pg. 33, middle); '. . . implemented in an instruction cache'(pg. 34, 2nd para), while the Disclosure is devoid of hardware or software in combination to corroborate to the fact that 'instruction cache' suddenly seems endowed with functionality of a processor, and according to known concept, this functionality without proper enabling support features, cannot be accepted, because cache is merely for storage of data or instructions just as memory is for read and write. The 'instruction cache' described as a functional capacity (from the above cited portions) therefore appears a far-fetched feature that cannot be construed as a specific feature that is possessed or invented by this Application, when commonly accepted meaning has it that 'instruction cache7 cannot exceed the connotation of a memory capacity; unless this cache is redefined by the Inventor to enable a proper understanding and recognition. Without which redefinition, that 'instruction cache' remains just for storage. The language as disclosed above amount to a language without specific and corroborated implementation facts; and what appears to be processor intelligence capacity from the disclosed 'instruction cache' is deemed not truly enabled.

Office Action dated December 21, 2007, pp. 6-7.

An instruction cache generally consists of the cache memory location, i.e., what the Examiner narrowly refers to as the cache, as well as a cache controller. However, both of these are needed to comprise "a cache." While any determination of the contents of instructions may technically be performed by the cache controller, the determination is still performed by "the cache." The Applicants submit that the Examiner's ultra-narrow definition of "a cache" is not consistent with the general usage of the term by one of ordinary skill in the art. Cache controllers are well known and enabled in the art, and thus the Specification, as written, is consistent with the known concept of "a cache."

However, in effort to expedite prosecution of the application, Applicants have amended the specification to address the Examiner's perceived informalities. In light of the amendments to the specification presented above, withdrawal of the objection is therefore respectfully requested.

IV. 35 U.S.C. § 112, Second Paragraph

The examiner has rejected claims 1, 2, 6, 26-48 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter, which applicants regard as the invention. This rejection is respectfully traversed.

Specifically, the Examiner states the following:

> The term "instruction cache" in claims 1, 32, 41 is used by the claim to mean "for receiving and for sending" while the accepted meaning is "special memory range or subsystem" (as in RAM) for storing of frequently accessed instructions. The term is indefinite because the specification does not clearly redefine the term. When interpreted in light of the Disclosure for determining and sending (see Specifications Objection), the above claim language amounts to a lack of

enablement impropriety, and an indefinite limitation that would enable one of ordinary skill in the art to make use of the Application.

Office Action dated December 21, 2007, pp. 7-8.

Applicants respectfully disagree with the Examiner. The term "instruction cache" is given its normal meaning. The Examiner acknowledges in the rejection that a cache can be a memory subsystem, but fails to recognize each component that is generally accepted to be included in that subsystem. A cache "subsystem" as the Examiner defines it, will also include a cache controller.

Additionally, Applicants point out that claim 1 is directed to "A method in a data processing system...." Similarly, claim 32 is directed to "A computer program product comprising... a computer readable, recordable-type medium having computer useable program code..." and claim 41 is directed to "A data processing system comprising... a processor unit [that]... executes the computer usable program code..." Nowhere do any of the claims recite that specific processes are performed by an instruction cache.

While the meaning of terms in the claims is controlled by the definitions presented in the specification, features from the specification may not be incorporated into the claims. *Toro Co. v. White Consolidated Industries Inc.*, 199 F.3d 1295, 1301, 53 USPQ2d 1065, 1069 (Fed. Cir. 1999) (meaning of words used in a claim is not construed in a "lexicographic vacuum, but in the context of the specification and drawings"). In reading the claims to require that an instruction cache to perform the operations specified, the Examiner has incorrectly imparted features of the specification into the claims.

In effort to expedite prosecution of the application, Applicants have amended the specification to address the Examiner's rejection. In light of the amendments to the specification presented above, withdrawal of the objection is therefore respectfully requested.

V. 35 U.S.C. § 101

The examiner has rejected claims 32-40 under 35 U.S.C. § 101 as being directed towards non-statutory subject matter. The Applicants have amended claim 32 as follows:

> 32. A computer program product comprising:
> a computer readable, recordable-type medium having computer useable program code for monitoring execution of instructions, the computer program product comprising:
> computer usable program code for receiving a bundle at an instruction cache, the bundle containing an instruction;
> computer usable program code for, responsive to receiving the bundle, determining whether the bundle contains an indicator, wherein the indicator identifies the instruction as one that is to be monitored by a performance monitor unit;
> computer usable program code for, responsive to a determination that the bundle contains the indicator, incrementing a counter associated with the

instruction wherein the incrementing provides a count of a number of times the instruction is executed; and

computer usable program code for, sending the bundle from the instruction cache to a functional unit for execution of the instruction.

Support for the claim amendments can be found on page 64 of the specification, as filed. Therein the Applicants define a recordable-type media as follows:

> Examples of computer readable media include recordable-type media, such as a floppy disk, a hard disk drive, a RAM, CD-ROMs, DVD-ROMs, and transmission-type media, such as digital and analog communications links, wired or wireless communications links using transmission forms, such as for example radio frequency and light wave transmissions.

Specification, p. 64.

Thus, by limiting the scope of claim 32 to recordable type media, the Applicant has excluded those forms of media which the Examiner rejects as non-statutory. Withdrawal of the rejection is therefore respectfully requested.

VI. 35 U.S.C. § 103, Obviousness

The examiner has rejected claims 1-2, 6, 26-48 under 35 U.S.C. § 103 as being unpatentable over *Gover* et al., Method and system for Performance Monitoring Through Monitoring an Order of Processor Events During Execution in a Processing System, U.S. Patent No. 5,752,062, (May 12, 1998) (hereinafter "*Gover*") in view of the Applicants' Specification. This rejection is respectfully traversed.

With regard to claim 1, the Examiner states the following:

> As per claim 1, Gover discloses a method in a data processing system for monitoring execution of instructions, the method comprising:
>
> receiving a bundle, the bundle containing an instruction (e.g. Fig. 1 ; Fig. 3);
>
> responsive to receiving the bundle, determining whether the bundle contains an indicator, wherein the indicator (see col. 7, lines 15 to col. 7, lines 17) identifies the instruction as one that is to be monitored by a performance monitor unit (Fig. 5);
>
> responsive to a determination that the bundle contains the indicator, incrementing a counter (e.g. Fig. 5; col. 7, line 62 to col. 8, line 17) associated with the instruction wherein the incrementing providing provides a count of a number of times the instruction is executed (see Fig. 6a, 6b); and
>
> sending the bundle to a functional unit for execution of the instruction (col. 4, lines 44- 49).
>
> Gover does not explicitly disclose 'instruction cache' unit that receives the bundle, determine the instruction to be counted based on the indicator for monitoring, and sending the bundle from the ICU to the execution unit; that is, not implementing the instruction cache, the sequence unit (see Fig. 1) and the monitoring unit (Fig. 2; Fig. 4; col. 7, lines 15 to col. 7, lines 17) in a combined

functional unit such as a single instruction cache unit (ICU). Gover discloses bus interface between instruction cache and sequencer unit (see Fig. 1 ; col. 6, lines 7-20); sequencer unit depending on rename buffer interface (col. 6, lines 13- 19); dispatching process including associating completion/allocation interfaces (e.g. Fig. 3) for updating information (or indicators) in a reorder buffer in terms of conditions (see finished, exception - col. 6, line 66, to col. 7, line 2) based on which some monitoring action (e.g. condition 2 - col. 10, line 9-12; dispatch logic 74 - Fig. 2; col. 7, lines 15 to col. 7, lines 17) can be applied; that is, using the performance monitor unit, in conjunction with the special registers or MMCRn (e.g. Fig. 4; Fig. 5; Fig. 6a). The meta-information being dispatched from the bundle of instructions coming from the reorder buffer, sequencer, rename buffer, and the tight relationship thereof with the original instruction cache (Fig. 1) and the performance monitor by Gover entails that the dispatched bundle contains instructions or data back and forth between cache and hardware monitoring tool. APA teaches combining hardware performance tools (Specifications, pg. 3) into a software application performance system or a trace tool using profiling. In view of the role played by the MMCRn and the sequencer, the cache interface unit, a rename process and the handling of runtime exception based on the hardware monitoring role as in Gover, i.e. the interdependency of functionality (hardware and software) units involved, it would have been obvious for one skill in the art at the time the invention was made to implement Gover's instruction cache, sequencer unit and monitoring unit (performance monitor 50, Fig. 4 4.e. hardware tools) as one functionality called instruction processing unit -- or more arbitrarily a 'instruction cache', or ICU- to effectuate a performance monitoring/support functionality such as contemplated by APA in terms of faster hardware performance. That is, one would be motivated to do so because this ICU can be called upon to receive bundle, trigger monitoring event based on indicators set forth by the reorder buffer inside the sequencer unit and provide expedite monitoring action (based on hardware support) operating on data from the dispatched bundle and based on the dynamic condition/state (e.g. exception, finished, completion) indicated by the bundle as set forth above (Fig. 6a, 6b) then accordingly send the bundle for execution after the appropriate monitoring action has taken place; and therefore enable the ICU to tackle problem based on state knowledge, e.g. completed state of an dispatched instructions (see col. 7, line 44 to col. 7, line 17; col. 15, line 36 to col. 16, line 22) in a timely manner without delays that would have resulted in cache miss (see col. 16, line 59 to col. 17, line 67)

Office Action dated December 21, 2007, pp. 10-12.

The Examiner bears the burden of establishing a *prima facie* case of obviousness based on prior art when rejecting claims under 35 U.S.C. § 103. *In re Fritch*, 972 F.2d 1260, 23 U.S.P.Q.2d 1780 (Fed. Cir. 1992). The prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka,* 490 F.2d 981, 180 USPQ 580 (CCPA 1974). In determining obviousness, the scope and content of the prior art are... determined; differences between the prior art and the claims at issue are... ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background the obviousness or non-obviousness of the subject matter is determined. *Graham v. John Deere Co.*, 383 U.S. 1 (1966). "Often, it will be necessary for a court to look to interrelated teachings of

multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *KSR Int'l. Co. v. Teleflex*, Inc., No. 04-1350 (U.S. Apr. 30, 2007). "Rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *Id.* (citing *In re Kahn*, 441 F.3d 977, 988 (CA Fed. 2006)).

Gover does not obviate the current claims because contrary to the Examiner's assertions, *Gover* does not disclose the claim feature of "responsive to receiving a bundle, determining whether the bundle contains an indicator, *wherein the indicator identifies the instruction as one that is to be monitored by a performance monitor unit*...." As explained in the prior office action response, *Gover* discloses:

> *Gover* describes an example of a trace technique similar to those known to the applicant and described as prior art on page 4 of the application as filed. These trace techniques are described as:
> periodically sampling a program's execution flows to identify certain locations in the program in which the program appears to spend large amounts of time. This technique is based on the idea of periodically interrupting the application or data processing system execution at regular intervals, so-called sample-based profiling. At each interruption, information is recorded for a predetermined length of time or for a predetermined number of events of interest. For example, the program counter of the currently executing thread, which is an executable portion of the larger program being profiled, may be recorded during the intervals. These values may be resolved against a load map and symbol table information for the data processing system at post-processing time, and a profile of where the time is being spent may be obtained from this analysis.

Specification, p. 4, ll. 3-19.

As described in *Gover*:

> a history of events is gathered in a processing system. The historical data is collected in a manner that is noninvasive to the system's operation but occurs within the processor. Thus, the data is unbiased and unaffected by external test instruments, while obtaining a cycle by cycle history of events during processing. Further, a straightforward manner of specifically choosing the instructions that initiate and complete monitoring activity is also obtained, which is normally more difficult in a processing system.

Gover, col. 3, ll. 44-52.

> Performance monitor 50, in a preferred embodiment, is a software-accessible mechanism intended to provide detailed information with significant granularity concerning the utilization of PowerPC instruction execution and storage control. Generally, the performance monitor 50 includes an implementation-dependent number (e.g., 2-8) of counters 51, e.g, PMC1-PMC8, used to count processor/storage related events.

Gover, col. 8, ll. 19-26.

> In operation, a notification signal is sent to PM 50 from time base facility 52 when a predetermined bit is flipped. The PM 50 then saves the machine state values in special purpose registers. In a different scenario, the PM 50 uses a "performance monitor" interrupt signalled by a negative counter (bit zero on or "1") condition.

Gover, col. 9, ll. 21-26.

In rejecting the claim feature "responsive to receiving a bundle, determining whether the bundle contains an indicator, *wherein the indicator identifies the instruction as one that is to be monitored by a performance monitor unit,*" the Examiner cites the following section of *Gover*:

> Referring also to FIG. 2, as dispatch logic 74 dispatches an instruction to an execution unit, sequencer unit 18 assigns the dispatched instruction to an associated entry in reorder buffer 76. Sequencer unit 18 assigns (or "associates") entries in reorder buffer 76 to dispatched instructions on a first-in first-out basis and in a rotating manner, such that sequencer unit 18 assigns entry 0, followed sequentially by entries 1-15, and then entry 0 again. As the dispatched instruction is assigned an associated entry in reorder buffer 76, dispatch logic 74 outputs information concerning the dispatched instruction for storage in the various fields and subfields of the associated entry in reorder buffer 76.
>
> For example, in entry 1 of FIG. 3, reorder buffer 76 indicates the instruction is dispatched to FXUA 22. In other significant aspects of the preferred embodiment, entry 1 further indicates the dispatched instruction has one GPR destination register (such that "number-of-GPR destinations"=1), has zero FPR destination registers (such that "number of-FPR destinations"=0), is not yet finished (such that "finished"=0), and has not yet caused an exception (such that "exception"=0).

Gover, col. 7, ll. 3-23.

Neither this section, nor elsewhere in *Gover* discloses the claim feature of "responsive to receiving a bundle, determining whether the bundle contains an indicator, *wherein the indicator identifies the instruction as one that is to be monitored by a performance monitor unit*…." This cited passage of *Gover* states that instructions are dispatched to a reorder buffer, and that the *reorder buffer* contains an indicator which indicates that the instruction has been dispatched. Again, nothing in the cited section or elsewhere discloses the claim feature of "responsive to receiving a bundle, determining whether the bundle contains an indicator, *wherein the indicator identifies the instruction as one that is to be monitored by a performance monitor unit*…."

Because *Gover* does not disclose at least the claim 1 feature of "responsive to receiving a bundle, determining whether the bundle contains an indicator, *wherein the indicator identifies the instruction as one that is to be monitored by a performance monitor unit,*" the Examiner has failed to state a *prima facie*

case of obviousness against claim 1. Therefore, the rejection of claim 1 under 35 U.S.C. § 103 has been overcome. Withdrawal of the rejection therefore requested.

Claims 6 and 26-31 depend from claim 1. The discussion of claim 1 above therefore applies to these dependent claims as well. By virtue of at least their dependence from claim 1, claims 6 and 26-31 are also not made obvious by *Gover*. In light of the reasons presented herein and the dependence of claims 6 and 26-31 from claim 1, the Examiner has failed to state a *prima facie* case of obviousness against claims 6 and 26-31. Therefore, the rejection of claims 6 and 26-31 under 35 U.S.C. § 103 has been overcome. Withdrawal of the rejection is therefore requested.

Independent claims 32 and 41 recite features similar to those found in claim 1. Therefore the reasons presented above in regard to claim 1's patentability over *Gover* are equally applicable to claims 32 and 41. In light of the reasons presented above in regard to claim 1, the Examiner has failed to state a *prima facie* case of obviousness against claims 32 and 41. Therefore, the rejection of claims 32 and 41under 35 U.S.C. § 103 has been overcome. Withdrawal of the rejection is therefore requested.

Claims 33-40 depend from claim 31. Claims 42-48 depend from claim 41. By virtue of at least their dependence from claim 31 and 41 respectively, claims 33-40 and claims 42-48 are also not made obvious by *Gover*. In light of the reasons presented herein and the dependence of claims 33-40 and claims 42-48 from their respective independent claims, the Examiner has failed to state a *prima facie* case of obviousness against claims 33-40 and claims 42-48. Therefore, the rejection of claims 33-40 and claims 42-48 under 35 U.S.C. § 103 has been overcome. Withdrawal of the rejection is therefore requested.

VII. Conclusion

It is respectfully urged that the subject application is patentable over *Gover* and is now in condition for allowance.

The examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

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